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PTO/SB/21 (04-04)

<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/781,334
	Filing Date	February 17, 2004
	First Named Inventor	Cameron McClintock
	Art Unit	2819
	Examiner Name	Don P. Le
	Attorney Docket Number	015114-052530US
Total Number of Pages in This Submission		

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to Technology Center (TC)
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
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<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Request for Refund	USPTO forms SB08A and SB08B (four pages), copies of 31 cited foreign patent and non-patent references, Return Postcard
<input checked="" type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> CD, Number of CD(s) _____	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<b>Remarks</b> The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.	
<input type="checkbox"/> Response to Missing Parts/Incomplete Application		
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Townsend and Townsend and Crew LLP Steven Cahill Reg. No. 44,578
Signature	
Date	7/30/04

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.			
Typed or printed name	Roger Hylton		
Signature		Date	7/30/04



PATENT  
Attorney Docket No.: 015114-052530US  
Client Reference No.: A518 D2

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Cameron McClintock et al.

Application No.: 10/781,334

Filed: February 17, 2004

For: I/O CELL CONFIGURATION FOR  
MULTIPLE I/O STANDARDS

Examiner: Don P. Le

Art Unit: 2819

INFORMATION DISCLOSURE  
STATEMENT UNDER 37 CFR §1.97 and  
§1.98

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:


The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the foreign patent and non-patent references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR §1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the

undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Steven Cahill", written in a cursive style.

Steven Cahill  
Reg. No. 44,578

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PTO/SB/08A (08-03)

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 4

**Complete if Known**

Application Number	10/781,334
Filing Date	February 17, 2004
First Named Inventor	Cameron McClintock
Art Unit	2819
Examiner Name	Don P. Le
Attorney Docket Number	015114-052530US

**U.S. PATENT DOCUMENTS+**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
	1	US-6,335,637	01-01-2002	Correale, Jr. et al.	
	2	US-6,229,365	05-08-2001	Iketani et al.	
	3	US-6,049,227	04-11-2000	Goetting et al.	
	4	US-6,040,712	03-21-2000	Mejia	
	5	US-6,018,252	01-25-2000	Imaizumi	
	6	US-5,974,476	10-26-1999	Lin et al.	
	7	US-5,815,013	09-29-1998	Johnston	
	8	US-5,798,659	08-25-1998	Shay et al.	
	9	US-5,612,637	03-18-1997	Shay et al.	
	10	US-5,589,783	12-31-1996	McClure	
	11	US-5,583,454	12-10-1996	Hawkins et al.	
	12	US-5,534,794	07-09-1996	Moreland	
	13	US-5,534,798	07-09-1996	Phillips et al.	
	14	US-5,521,530	05-02-1996	Yao et al.	
	15	US-5,440,249	08-08-1995	Schucker et al.	
	16	US-5,428,305	06-27-1995	Wong et al.	
	17	US-5,428,800	06-27-1995	Hsieh et al.	
	18	US-Re. 34,808	12-20-1994	Hsieh	
	19	US-5,374,858	12-20-1994	Elmer	
	20	US-5,369,317	11-29-1994	Casper et al.	
	21	US-5,332,935	07-26-1994	Shyu	
	22	US-5,317,210	05-31-1994	Patel	
	23	US-5,311,080	05-10-1994	Britton et al.	
	24	US-5,300,835	04-05-1994	Assar et al.	
	25	US-5,282,271	01-25-1994	Hsieh et al.	
	26	US-5,235,219	08-10-1993	Cooperman et al.	
	27	US-5,151,619	09-29-1992	Austin et al.	
	28	US-5,132,573	07-21-1992	Tsuru et al.	
	29	US-5,034,634	07-23-1991	Yamamoto	
	30	US-5,028,821	07-02-1991	Kaplinsky	
	31	US-5,023,488	06-11-1991	Gunning	
	32	US-4,999,529	03-12-1991	Morgan, Jr. et al.	
	33	US-4,994,691	02-19-1991	Naghshineh	
	34	US-4,987,319	01-22-1991	Kawana	
	35	US-4,975,602	12-04-1990	Nhu	
	36	US-4,970,410	11-13-1990	Matsushita et al.	
	37	US-4,933,577	06-12-1990	Wong et al.	
	38	US-4,879,481	11-07-1989	Pathak et al.	
	39	US-4,820,937	04-11-1989	Hsieh	
	40	US-4,797,583	01-10-1989	Ueno et al.	
	41	US-4,791,312	12-13-1988	Weick	

Examiner  
SignatureDate  
Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Kind Codes of U.S. Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>			<b>Complete if Known</b>		
			Application Number	10/781,334	
			Filing Date	February 17, 2004	
			First Named Inventor	Cameron McClintock	
			Art Unit	2819	
Examiner Name	Don P. Le				
Sheet	2	of	4	Attorney Docket Number	015114-052530US

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
	42	US-4,783,607	11-08-1988	Hsieh	
	43	US-4,742,252	05-03-1988	Agrawal	
	44	US-4,625,129	11-25-1986	Ueno	
	45	US-4,527,079	07-02-1985	Thompson	
	46	US-4,472,647	09-18-1984	Allgood et al.	
	47	US-4,469,959	09-04-1984	Luke et al.	
	48	US-4,032,800	06-28-1977	Droscher et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
	49	EP	0 358 501	A2	14-03-1990	Kawasaki Steel		<input type="checkbox"/>
	50	EP	0 426 283	B1	29-12-1997	SGS Thompson		<input type="checkbox"/>
	51	EP	0750242	A2	12-27-1996	Fujitsu Ltd.		<input type="checkbox"/>
	52	EP	0718977	A2	06-26-1996	ST Microelectronics		<input type="checkbox"/>
	53	EP	0 616 431	A1	21-09-1994	AMD		<input type="checkbox"/>
	54	EP	0 608 515	A1	03-08-1994	Motorola		<input type="checkbox"/>
	55	EP	0 544 461	A1	02-06-1993	AT&T		<input type="checkbox"/>
	56	JP	04-223617		08-13-1992	Ricoh		abstract only
	57	JP	02-161820		06-21-1990	Kawasaki		abstract only
	58	JP	02-013124		01-17-1990	Kawasaki		abstract only
	59	JP	01-274512		11-02-1989	Hitachi		abstract only
	60	PCT	WO98/47230		10-22-1998	Xilinx, Inc.		<input type="checkbox"/>

Examiner Signature		Date Considered	
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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/781,334
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				First Named Inventor	Cameron McClintock
				Art Unit	2819
				Examiner Name	Don P. Le
Sheet	3	of	4	Attorney Docket Number	015114-052530US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	61	Altera Corporation, Data Sheet, "Flex 10K Embedded Programmable Logic Family," Jul., 1995, ver. 1, pp. 1-39.	
	62	Altera Corporation, Data Sheet, "Apex 20K", May, 1999, pp. 23-88.	
	63	CHAPPELL et al. "Fast CMOS ECL Receivers With 100-mV Worst-Case Sensitivity," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 23, No. 1, February 1988, pp. 59-66.	
	64	CLAUDE "Cross-boundary PLDs," <i>Semiconductor Currents</i> , June 1991, pp. 9-10.	
	65	GUARDIANI et al. "Applying a submicron mismatch model to practical IC design," <i>IEEE 1994 Custom Integrated Circuits Conference</i> , 1994, pp. 297-300.	
	66	GUNNING et al., "A CMOS Low-Voltage-Swing Transmission-Line Transceiver," <i>IEEE International Solid-State Circuits Conference</i> , 1992, pp. 58-59.	
	67	HAINES "Field-programmable gate array with non-volatile configuration," <i>Microprocessors and Microsystems</i> , Vol. 13, No. 5, June 1989, pp. 305-312.	
	68	HANAFI et al. "Design and Characterization of CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 27, No. 5, May 1992, pp. 783-785.	
	69	MARTINEZ "IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications," National Semiconductor Application Note 829, June 1992, pp. 1-5.	
	70	KNACK "Debunking High-Speed PCB Design Myths," <i>ASIC &amp; EDA</i> , July 1993, pp. 12-26.	
	71	PELGROM et al. "A 3/5 V Compatible I/O Buffer," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 30, No. 7, July 1995, pp. 823-825.	
	72	PELGROM et al. "Matching Properties of MOS Transistors," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 5, October 1989, pp. 1433-1440.	
	73	PRINCE et al. "ICs going on a 3-V diet," <i>IEEE Spectrum</i> , May 1992, pp. 23-25.	
	74	ROBERTS et al. "Session XIX: High Density SRAMs," <i>IEEE International Solid-State Circuits Conference</i> , February 27, 1987, pp. 252-254.	
	75	SENTHINATHAN et al., "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 28, No. 12, December 1993, pp. 1383-1388.	
	76	SENTHINATHAN et al., "Simultaneous Switching Ground Noise Calculation for Packaged CMOS Devices," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 26, No. 11, November 1991, pp. 1724-1728.	

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	77	UEDA et al. "A 3.3V ASIC for Mixed Voltage Applications With Shut Down Mode," <i>IEEE 1993 Custom Integrated Circuits Conference</i> , May 9-12, 1993, pp. 25.5.1 to 25.5.4.	
	78	VOLDMAN "ESD Protections in a Mixed Voltage Interface and Multi-Rail Disconnected Power Grid Environment in 0.50- and 0.25- $\mu$ m Channel Length CMOS Technologies," <i>EOS/ESD Symposium</i> , 1994, pp. 3.4.1 to 3.4.10.	
	79	VU et al. "A Gallium Arsenide SDFL Gate Array with On-Chip RAM," <i>IEEE Journal of Solid-State Circuits</i> , Vol. sc-19, No. 1, February 1984, pp. 10-22.	
	80	WILLIAMS "Mixing 3-V and 5-V ICs," <i>IEEE Spectrum</i> , March 1993, pp. 40-42.	

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